IN THE CLAIMS

Please amend the claims as follows:

1. (original) A switch circuit (10) comprising:

- at least two input terminals (20, 22) and one output terminal (24),
- first switches (28, 30), each comprising a first and second port (44, 46), said first switches (28, 30) being electronically switchable between a first state, where there is a high insertion loss between the first and second ports (44, 46), and a second state, where there is a low insertion loss between the first and second ports (44, 46), where each of the input terminals (20, 22) is connected to a first port (44) of one of said first switches (28, 30),
- and a second switch (32) with at least two branch ports (48, 50) and a common port (52), said second switch (32) electronically switchable between different states, where in each state the insertion loss between one branch port (48, 50) and the common port (52) is low, while the insertion loss between the common port (52) and the other branch port (48, 50) is high,
- where each of the branch ports (48, 50) is connected to a second port (46) of one of said first switches (28, 30).

2. (original) Circuit according to claim 1, where the first switches (28, 30) are implemented using PIN diodes (D1, D2).

3. (original) Circuit according to claim 2, where

- first switches (28, 30) are implemented using two anti-parallel PIN-diodes (D1, D2) in series connection between first and second ports (44, 46),
- and a driver terminal (56) is connected between the diodes (D1, D2).

4. (currently amended) Circuit according to ~~one of the above claims~~claim 1, where the first switches (28, 30) are comprised of discrete electronic parts.

5. (currently amended) Circuit according to ~~one of the above claims~~claim 1, where the second switch (32) is an integrated circuit.

6. (currently amended) Circuit according to ~~one of the above claims~~claim 1, where a control circuit (34) is provided to synchronously control first and second switches (28, 30, 32).

7. (currently amended) Circuit according to ~~one of the above claims~~claim 1, where

- a control circuit (34) is provided comprising a control terminal (38) and at least two driver circuits (40, 42),
- where a first driver circuit (40) provides an in-phase voltage signal (V_{SW}) to drive one of the first switches (30), and
- where the second driver circuit (42) provides an inverted voltage signal ($\underline{V}_{SW}$) to drive another of the first switches (28).

8. (currently amended) Circuit according to one of claim 6~~ or 7~~, where the control circuit (34) is connected to an I2C transceiver (36).

9. (currently amended) A receiver circuit for receiving a radio frequency signal, comprising

- at least two radio frequency input terminals,
- a tuner circuit (12) for receiving radio frequency signals at an input, and for generating baseband signals,
- and a switch circuit (10) according to ~~one of the preceding claims~~claim 1, where the input terminals (20, 22) are connected to the radio frequency inputs and the output terminal (24) is connected to the input of the tuner (12).